ABSTRACT

0030 A method for forming a copper dual damascene with improved copper migration resistance and improved electrical resistivity including providing a semiconductor wafer including upper and lower dielectric insulating layers separated by a middle etch stop layer; forming a dual damascene opening extending through a thickness of the upper and lower dielectric insulating layers wherein an upper trench line portion extends through the upper dielectric insulating layer thickness and partially through the middle etch stop layer; blanket depositing a barrier layer including at least one of a refractory metal and refractory metal nitride to line the dual damascene opening; carrying out a remote plasma etch treatment of the dual damascene opening to remove a bottom portion of the barrier layer to reveal an underlying conductive area; and, filling the dual damascene opening with copper to provide a substantially planar surface.